TO THE ASSISTANT COMMISSIONER FOR PATENTS:

In the Drawings:

The Applicant respectfully requests the Examiner to transfer FIGS. 1, 1a, and 3 - 6 from the file of the issued `709 patent to the reissue file, and requests approval of the amendment to FIG. 2 as requested in the enclosed Request for Drawing Change.

In the Specification:

In the Abstract, line 8, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Lines 9 – 10, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Starting in column 1, line 6, through column 2, line 6, please insert:

--[The subject matter of the present application is related to copending U.S. application Ser. No. 08/173,197, filed Dec. 22, 1993, titled "Improved Static Memory Long Write Test", attorney docket no. 93-C-82, copending U.S. application Ser. No. 08/172,854, filed Dec. 22, 1993, titled "Stress Test Mode", attorney docket no. 93-C-56 all of which are assigned to SGS-Thomson Microelectronics, Inc. and expressly incorporated herein by reference.

Additionally, the following pending U.S. patent applications by David Charles McClure entitled:

"Architecture Redundancy", Ser. No. 08/582,484 (Attorney's Docket No. 95-C-136), and

"(Redundancy Control", Ser. No. 08/580,827 (Attorney's Docket No. 95-C-143), which were both filed on Dec. 29, 1995, and have the same ownership as the present application, and to that extent are arguable related to the present application, which are herein incorporated by reference;

and entitled:

"Test Mode Activation and Data Override", Ser. No. 08/587,709 (Attorney's Docket No. 95-C-137),

"Pipelined Chip Enable Control Circuitry and Methodology", Ser. No. 08/588,730_(Docket No. 95-C-138),

"Output Driver Circuitry Having a Single Slew Rate Resistor", Ser. No. 08/588,988 (Docket No. 95-C-139),

"Synchronized Stress Test Control", Ser. No. 08/589,015 (Docket No. 95-C-142),

"Write Pass Through Circuit", Ser. No. 08/588,662 (Attorney's Docket No. 95-C-144), "Data-Input Device for Generating Test Signals on Bit and Bit-Complement Lines", Ser. No. 08/588,762 (Attorney's Docket No. 95-C-145),

"Synchronous Output Circuit", Ser. No. 08/588,901 (Attorney's Docket No. 95-C-146),

"Write Driver Having a Test Function", Ser. No. 08/589,141 (Attorney's Docket No. 95-C-147),

"Circuit and Method for Tracking the Start of a Write to a Memory Cell", Ser. No. 08/589,139 (Attorney's Docket No. 95-C-148),

"Circuit and Method for Terminating a Write to a Memory Cell", Ser. No. 08/588,737 (Attorney's Docket No. 95-C-149),

"Clocked Sense Amplifier with Wordline Tracking", Ser. No. 08/587,728 (Attorney's Docket No. 95-C-150),

"Memory-Row Selector Having a Test Function", Ser. No. 08/589,140 (Attorney's Docket No. 95-C-151),

"Device and Method for Isolating Bit Lines from a Data Line", Ser. No. 08/588,740 (Attorney's Docket No. 95-C-154),

"Circuit and Method for Setting the Time Duration of a Write to a Memory Cell", Ser. No. 08/587,711 (Attorney's Docket No. 95-C-156),

"Low-Power Read Circuit and Method for Controlling A Sense Amplifier", Ser. No. 08/589,024, U.S. Pat. No. 5,619,466 (Attorney's Docket No. 95-C-168),

"Device and Method for Driving a Conductive Path with a Signal", Ser. No. 08/587,708 (Attorney's Docket No. 169),

and the following pending U.S. patent applications by Mark A. Lysinger entitled:

"Burst Counter Circuit and Method of Operation Thereof", Ser. No. 08/589,023 (Attorney's Docket No. 95-C-141),

"Switching Master/Slave Circuit", Ser. No. 08/588,648 (Attorney's Docket No. 96-C-03),

which have the same effective filing data and ownership as the present application, and to that extent are arguably related to the present application, are incorporated herein by reference.]

The subject matter of the present application is related to U.S. Pat. No. 5,577,051, titled "Improved Static Memory Long Write Test", U.S. Pat. No. 5,835,427, titled "Stress Test Mode", all of which are assigned to SGS-Thomson Microelectronics, Inc. and expressly incorporated herein by reference.

Additionally, the following U.S. patents by David Charles McClure entitled:

"Architecture Redundancy", U.S. Pat. No. 5,612,918, and

"Redundancy Control", U.S. Pat. No. 5,790,462, which were both filed on Dec. 29, 1995, and have the same ownership as the present application, and to that extent are arguably related to the present application, which are herein incorporated by reference;

and entitled:

"Test Mode Activation and Data Override", Ser. No. 08/587,709,

Ser. No. 09/457,558 which is a continuation of Ser. No. 08/587,709,

Ser. No. 09/454,800 which is a divisional of Ser. No. 08/587,709,

"Pipelined Chip Enable Control Circuitry and Methodology", U.S. Pat. No. 5,701,275,

U.S. Pat. No. 5,798,980 which is a divisional of U.S. Pat. No. 5,701,275,

"Output Driver Circuitry Having a Single Slew Rate Resistor", U.S. Pat. No. 5,801,563,

"Synchronized Stress Test Control", U.S. Pat. No. 5,712,584,

"Write Pass Through Circuit", U.S. Pat. No. 5,657,292,

"Data-Input Device for Generating Test Signals on Bit and Bit-Complement Lines", U.S. Pat. No. 5,845,059,

"Synchronous Output Circuit", U.S. Pat. No. 5,619,456,

"Write Driver Having a Test Function", U.S. Pat. No. 5,745,432,

"Circuit and Method for Tracking the Start of a Write to a Memory Cell", Ser. No. 08/589,139 (since abandoned),

U.S. Pat. No. 5,808,960 which is a continuation of Ser. No. 08/589,139,

"Circuit and Method for Terminating a Write to a Memory Cell", Ser. No. 08/588,737 (since abandoned),

U.S. Pat. No. 5,825,691 which is a continuation of Ser. No. 08/588,737,

"Clocked Sense Amplifier with Wordline Tracking", U.S. Pat. No. 5,802,004,

U.S. Pat. No. 5,828,622 which is a divisional of U.S. Pat. No. 5,802,004,

"Memory-Row Selector Having a Test Function", Ser. No. 08/589,140 (since abandoned),

U.S. Pat. No. 5,848,018 which is a continuation of Ser. No. 08/589,140,

"Device and Method for Isolating Bit Lines from a Data Line", U.S. Pat. No. 5,691,950,

"Circuit and Method for Setting the Time Duration of a Write to a Memory Cell", U.S. Pat. No. 5,864,696,

U.S. Pat. No. 6,006,339 which is a divisional of U.S. Pat. No. 5,864,696,

"Low-Power Read Circuit and Method for Controlling A Sense Amplifier", U.S. Pat. No. 5,619,466,

"Device and Method for Driving a Conductive Path with a Signal", Ser. No. 08/587,708 (since abandoned),

U.S. Pat. No. 5,896,336 which is a continuation of Ser. No. 08/587,708,

U.S. Pat. No. 5,883,838 which is a divisional of Ser. No. 08/587,708,

and the following U.S. patents by Mark A. Lysinger entitled:

"Burst Counter Circuit and Method of Operation Thereof", Ser. No. 08/589,023 (since abandoned),

U.S. Pat. No. 5,805,523 which is a continuation of Ser. No. 08/589,023,

"Switching Master/Slave Circuit", U.S. Pat. No. 5,783,958,

which have the same effective filing data and ownership as the present application, and to that extent are arguably related to the present application, are incorporated herein by reference.--

In column 3, line 3, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Line 5, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Line 51, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Line 53, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Line 60, please replace "and then are allowed to sequentially conduct" with --[and then are allowed to sequentially conduct]--.

In column 4, line 35, please replace "Control bar signal **14** and Control signal **18**" with --Control bar derivative signal [**14**]**23 from Node 4** and Control derivative signal [**18**]**27 from node 3**--.

Line 39, please replace "**14**" with --[**14**]**23**--.

Line 42, please replace "**18**" with --[**18**]**27**--.

Line 49, please replace "**23**" with --[**23**]**21**--.

Line 67, please replace "signal" with --derivative signal--.

In column 5, line 1, please replace "**3**" with --[**3**]**4**--, "signal" with --derivative signal--, and "**4**" with --[**4**]**3**.

Line 4, after "Conversely," please insert -- when the Power-On-Reset signal **16** goes to a low logic state, and--.

Line 5, please replace both instances of "signal" with --derivative signal—and please replace "go to" with –[go to]remain at--.

Line 9, please replace both instances of "signal" with --derivative signal--.

Line 14, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 19, please replace "which is allowed to device conduct" with --[which is allowed to device conduct]--.

Line 20, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 24, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 33, please replace "passgate" with --passgates 90 and--.

Line 34, please insert --derivative-- before "signal".

Line 36, please replace "13" with --[13]21--.

Line 40, please insert --derivative-- before both instances of "signal".

Line 43, please replace "high" with --[high]low--.

Line 44, please replace "**12**" with --[**12**]**38**-- and "turning off" with --[turning off]thus latching--.

Line 52, please replace "inverter" with --[inverter]invert--.

Line 64, after "Address", please insert --bar--, and please replace "116" with --[116]128--.

Line 66, after "Address", please insert --bar--, and please replace "116" with --[116]128--.

In column 6, line 32, after "transistors" please insert --**158**.--.

Line 27, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 35, please replace "**152**" with --[**152**]**162**--.

Line 36, please replace "**152**" with --[**152**]**162**--.

Line 55, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 59, please replace "signal **12**" with --derivative signal [**12**]**38**--.